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Evolution of the Command Subsystem for the Nimbus Family of Satellites

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Summary

There are four satellites included in the NIMBUS spacecraft family. Two satellites have been launched, the third is about to be launched, and the fourth is presently being developed for launch in 1969. A Command Clock Subsystem is part of every NIMBUS Satellite, and each satellite has a Command Clock Subsystem which differs with its predecessor. A discussion of the differences among the Command Clock Subsystems is the purpose of this paper.

Introduction

The NIMBUS family of satellites is used to support meteorological research and development. Included in this family are the NIMBUS A, C, B, and D spacecrafts, which appear in that order. All NIMBUS spacecrafts have been designed and developed under the management of NASA's Goddard Space Flight Center. The function of the spacecrafts is to serve as orbiting test beds for instrumentation to collect weather data and perform other scienfitic experiments. Subsystems, other than experiments, are provided on the spacecraft to aid and control the experiments. These subsystems, among others, are used to provide attitude control, primary power, telemetering, data recording, transmitting, command control, and reference frequencies.

Many organizations have collaborated in developing the various subsystems for the NIMBUS satellites. Although each subsystem was developed in accordance with specific individual requirements, all had to meet the design objectives of survival under severe environmental stresses during launch and at least six months operation in orbit. For NIMBUS D, the design goal for operation in orbit is a minimum of one year. California Computer Products, Inc. (CalComp) has been involved in the NIMBUS program since 1960.

CalComp's responsibility has been the design and development for all of the Command Clock Subsystems used in the NIMBUS spacecrafts. Each succeeding Command Clock Subsystem provided more capability than its predecessor. Although each Command Subsystem's external function is similar, it is the internal mechanization and increased functional capability that varies.

General

The command data link includes a Ground Station, Receiver, and Command Clock. The Ground Station transmits the data to the spacecraft receiver which demodulates, detects, and sends binary data bits on three channels to the Command Clock for decoding and processing. The Ground Station data to be sent to the Command Subsystem is processed by frequency modulating three subcarriers and then transmitted to the spacecraft by amplitude modulation. Four additional amplitude-modulated subcarriers are transmitted to perform emergency control. For NIMBUS D, the four individual subcarriers are added in pairs, before being amplitude-modulated, to provide six commands for emergency purposes. It is through this Ground Station to spacecraft data link that control of all instrumentation on board the spacecraft is achieved. During the course of developing the different Command Clock Subsystems, there have been refinements to increase the reliability and functional capability of each. The increased performance was necessary as each spacecraft added more instrumentation, thus, requiring more control with greater reliability.

The basic operation of each Command Clock Subsystem is similar in that they provide precision frequency outputs for experiment synchronization, stored commands for delayed command executions during the course of an orbit, real time and time code modulated outputs for information correlation, and relay matrix drivers for satellite subsystems control. The input/output functions of each Command Clock Subsystem are similar in function but differ in quantity. A comparison of the input/output functions and quantity for each Command Clock Subsystem is shown in Table 1.

NIMBUS A Command Clock Subsystem

The NIMBUS A Spacecraft was the first of the series. It was launched in autumn 1964. Its orbital life lasted approximately one month. The failure was due to a power lost because the solar cell panels could not be controlled to keep them oriented toward the sun. The bearings in the motors to drive the solar cell panels froze, making panel positioning inoperative.

While on board the NIMBUS A Spacecraft, the Command Clock performed its functions well.

TABLE 1

Input-Output Functions for NIMBUS Satellite

Command Clock Subsystems

Input-Output Function	NIMBUS A	NIMBUS C	NIMBUS B (Two Command Clocks Plus Interface Box)	NIMBUS D
Inputs Data Input Channels	(3) Data, Strobe, and Character Sync	(3) Data, Strobe, and Character Sync	(6) Data, Strobe, and Character Sync	(3) Data, Strobe, and Message Duration
Keying Inputs	*N/A	4 - Keying Plug	8 - Keying Plug	32 - Keying Plug
Data Code Sync Pulse	*N/A	1 - Initialize Data Code	*N/A	*N/A
Outputs Frequency Amplifiers	(20) 1Hz, 10Hz, 400Hz, 500Hz, 2400Hz, 5kHz, 10kHz, 400kHz	(19) 1Hz, 10Hz, 500Hz, 2400Hz, 5kHz, 200kHz,	(18) 1Hz, 10Hz, 500Hz, 2400Hz, 5kHz, 200kHz, 1.6mHz	(40) 1Hz, 10Hz, 500Hz, 1kHz, 2kHz, 2.4kHz, 2.5kHz, 5kHz, 10kHz, 50kHz, 200kHz, 400kHz, 1.6mHz
Synchronous Motor Drives	(20) 100Hz - 2 phase 400Hz - 2 phase	(20) 100Hz - 2 phase 400Hz - 2 phase	(20) 100Hz - 2 phase 400Hz - 2 phase	(20) 100Hz - 2 phase (low level) 400Hz - 2 phase (high Level)
Time Code	(3) Modulated 10Hz, 50kHz	(5) Modulated 10Hz, 50kHz Minitrack PDM/NRZ	(4) Modulated 2.5kHz, 10kHz Minitrack PDM	(5) Modulated 2.5kHz, 10kHz PDM, Strobe
Matrix Lines	(24) 8 Rows - 16 Columns 128 Commands	(24) 8 Rows - 16 Columns 128 Commands	(48) (8 Rows - 16 Columns) x 2 170 Commands (some are redundant)	(46) 16 Rows - 30 Columns 480 Commands
Data Code and Grid	*N/A	(2) Data Code Word 1/8 Hz Signal	*N/A	*N/A
Telemetry Points	31	30	28	54
Serial Data Transfer	*N/A	*N/A	*N/A	3 Mode, Data, Strobe

*N/A - Not Applicable

It interfaced with three experiments plus the other service-type subsystems to provide them with timing and command signals.

The operation of this subsystem can best be explained with the aid of the block diagram shown in Figure 1.

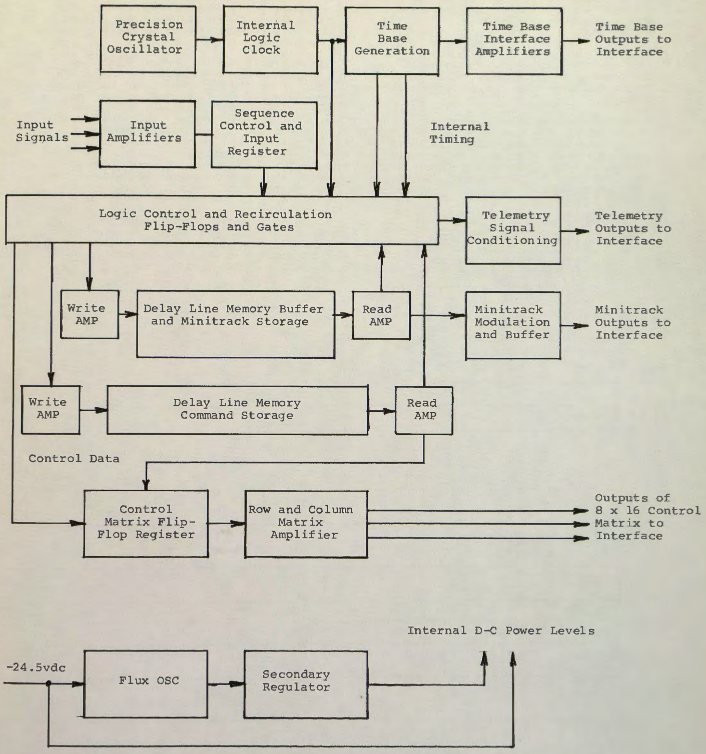


FIGURE 1

NIMBUS A Command Clock Subsystem
Functional Block Diagram

The basic operational parts of the Command Clock other than the power supply, drivers, and telemetry networks are a precision crystal oscillator, time-based generation, delay line memories, control matrix flip-flop register, and the relay matrix drivers. The oven-controlled precision crystal oscillator provided an 800-kHz signal which was stable to 1 part in 10^7. The oscillator drove an internal pulse generator which clocked all the flip-flops in the Command Subsystem. The time-based generator consisted of a series of flip-flops to divide the 800-kHz signal to provide various reference frequencies at the interface. Each frequency exhibited the same relative precision due to its common origin.

Three input channels were required to communicate with the Command Subsystem. The three channels provided data bits, bit synchronization, and parity bit synchronization. Figure 2 shows the relationship among the three input channels which are designated as the W, X, and Y signals.

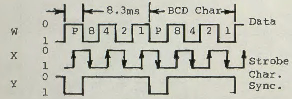


FIGURE 2
NIMBUS A Command Clock Input Channels Waveform Relationship

As can be seen, the W channel carried the command information in the form of a 5-bit character transmitted NRZ (non-return-to-zero); four bits contained the data, and the fifth bit contained the odd parity indication. The maximum data rate was 120 bits per second. The X and Y channels were timing signals to ensure synchronization of the satellite clock. The X signal was a reference square wave 90 degrees out of phase with W, and Y was a character sync channel with a pulse marking the parity bit time of the channel.

The data word for the Command Clock Subsystem consisted of 12 BCD characters (48 bits). The first character was a flag character for satellite identification. The next ten characters were data characters, indicating time or indicating a command instruction with time of execution. The last character was an ENTER code to store the data into the command storage delay line. Each command was transmitted twice; the second command was rejected if the first entered the stored command memory correctly. As each character was received by the Command Clock, it was processed through the timer delay line memory where the message was parity checked and stored until a full word was received. The timer memory was divided into four sectors as shown in Figure 3.

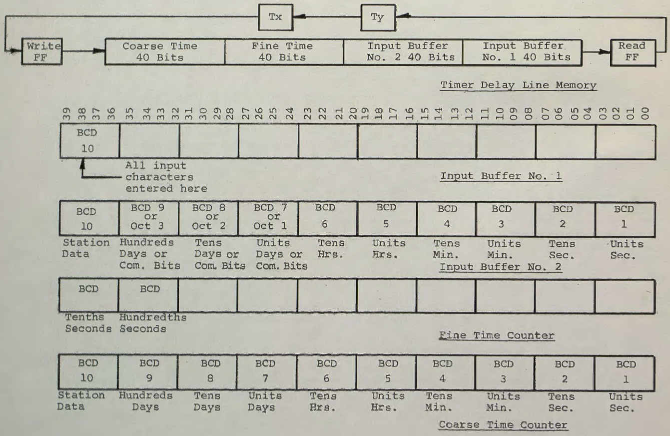


FIGURE 3

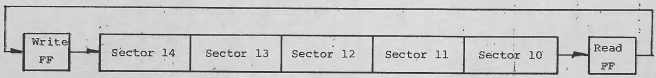
Timer Delay Line Memory Sectors

Two sectors served as input buffer registers. The third sector was a real time counter capable of being updated by command. The fourth sector, designated the fine time counter, served as a divider of the 100-Hz signal to provide a 1-Hz signal output.

The Buffer No. 1 register held each character until parity checked. The character was then shifted into the Buffer No. 2 register where the ten data characters were collected before being transferred to the command storage delay line memory shown in Figure 4. The information was stored in the command storage delay line location designated by the ENTER code. There were five different ENTER codes, one for each command storage memory location.

The command storage memory contained information on what command was to be executed and the time of execution. Each word of the stored command had its time of execution compared with the coarse time counter in the timer loop. When agreement occurred, the command was gated into the control matrix flip-flop register where it was decoded to select the appropriate column and row drivers of the relay matrix drivers. Since it had an 8 x 16 matrix, the Command Clock was capable of executing 128 different commands. The duration of the command execution was 68 milliseconds. All five storage commands could be executed within a minimum time of five seconds or be delayed up to 24 hours.

Aside from the frequency outputs, telemetry outputs, and command outputs, the Command Clock Subsystem transmitted a Minitrack time code output which contained the clock real-time information. This output was a continuous pulse-width modulated (PWM) signal divided into ten 100-millisecond intervals, representing a real time. Figure 5 shows the Minitrack Time Code Format.



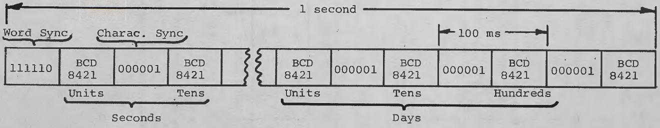
Capacity - 200 bits

Circulation - 800 kHz

Bit Time - 1.25 μsec

FIGURE 4

Stored Command Delay Line Memory



One bit = 10 ms

FIGURE 5

Minitrack Time Code Format

TABLE 2

Physical Characteristics of NIMBUS Satellite
Command Clock Subsystems

Physical Characteristics	NIMBUS A	NIMBUS C	NIMBUS B	NIMBUS D
Packaging Construction	One Box Nickel-plated, machined case of cast magnesium alloy. Covers are flat stock.	One Box Nickel-plated, machined case of cast magnesium alloy. Covers are flat stock.	Three Boxes Nickel-plated, machined case of cast magnesium alloy. Covers are flat stock.	1 Box Nickel-plated machined magnesium alloy, flat stock.
Size	6" W x 8" D x 13" H Volume: 0.36 cu. ft.	6" W x 8" D x 13" H Volume: 0.36 cu. ft.	2 Boxes: 6"Wx8"Dx13"H 1 Box: 6"Wx8"Dx6.5"H Volume: 0.90 cu. ft.	6" W x 8" D x 13" H Volume: 0.36 cu. ft.
Weight	18 pounds	20 pounds	Total Subsystem 51.1 pounds	Approximately 22 pounds
Components	Discrete components, diode logic gates	Discrete components, diode logic gates	Discrete components, diode logic gates, mechanical relays	Integrated circuits MOS registers, hybrid circuit flat packs, discrete components, relays
Printed Circuits	Two sided: components mounted on one side only -- 23 boards	Two sided: components mounted on one side only -- 23 boards	Two sided: components mounted on one side only -- 58 boards	Multilayer ribbon cable interconnections 8 boards plus power supply
Memory Device	2 delay lines 5 stored commands	2 delay lines 11 stored commands	4 delay lines (2 each command clock) 32 stored commands	32 MOS shift registers 30 stored commands
Environment	NASA Specification for NIMBUS Clock Subsystem Nov. 1960	NASA Environmental Specification for Meteorological Spacecraft Subsystem Apr.1964	NASA Specification S-320-NI-2 Nov. 16, 1966	NASA Specification S-320-NI-3A September 22, 1967
Reliability	Non-Redundant MTBF: 6 months (orbit)	Non-Redundant MTBF: 6 months (orbit)	Dual Redundant Clocks OR'd through Interface Box MTBF: 6 months (orbit)	Selective Redundancy MTBF: 1 year (orbit)
Power Input (nominal)	-24.5v ± 5 percent	-24.5v ± 5 percent	-24.5v ± 5 percent	-24.5v ± 5 percent

This time code was made available to the other subsystems in the satellite in serial fashion. The NIMBUS A Command Clock Subsystem generated two other Minitrack outputs. These were coherent 10-kHz and 50-kHz carriers amplitude modulated by the Minitrack binary time code.

Information pertaining to the physical characteristics of the NIMBUS A Command Subsystem is shown in Table 2.

NIMBUS C Command Clock Subsystem

The NIMBUS C spacecraft was launched on 15 May 1966. As of this writing, some of its subsystems have stopped operating, but others are still functioning to provide useful weather data. For the most part, the satellite has exceeded its operational goal of six months in orbit and the Command Clock Subsystem on board is one of the subsystems still operating.

The NIMBUS C Command Clock Subsystem interfaced with four experiments. Its operation is the same as that of NIMBUS A except that it had an increase in its output capacity as indicated in Table 1. In addition to its output capability increase, it also had some refinements in its internal logical operation. The NIMBUS A Command Clock Subsystem block diagram shown in Figure 1 is still applicable for describing the operation of the NIMBUS C Command Clock Subsystem; however, changes have been made within the blocks. The most significant changes have been the replacement of the 800-kHz signal source with a 3.2-mHz oven-controlled crystal oscillator. The reason for the increased frequency is that the 3.2-mHz crystal oscillator exhibited more stability as crystals are more suitable for operation at the higher frequencies. Another change in the NIMBUS C internal mechanization was the increase in the amount of storage in both the timer and command storage delay line memories. An additional word was added to the timer memory, and 11 words were added to the command storage memory. The new word added to the timer memory was used as a data output buffer register. Besides the addition of this output buffer, additional functions were implemented in the input buffer No. 1 and the fine time-counter registers. Figure 6 shows the configuration of the timer memory.

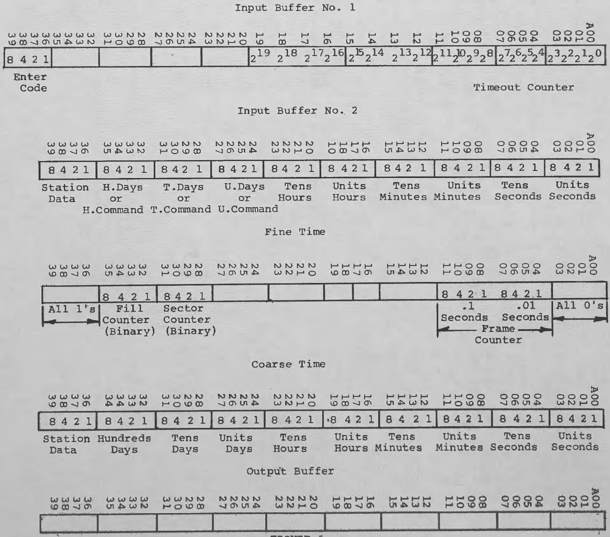


FIGURE 6

NIMBUS C Command Clock Timer Delay Line Registers

Input buffer No. 1 register contained a binary "timeout" counter which determined the time duration since the last Ground Station command access, and issued two command matrix timeout commands for emergency purposes if the duration exceeded nine hours. Other functions of the buffer No. 1 register are the same as for the buffer in the NIMBUS A Command Clock Subsystem. The input buffer No. 2 register performed the same function as it did in NIMBUS A.

The fine time counter register was changed. In addition to containing the counter which divided the 100-Hz signal to a 1-Hz signal, it also contained four other counters. These were a 6-bit binary counter to divide a 1-Hz signal by 40 for establishing the data code output word length; a 4-bit binary readout counter whose setting determined which of the 16 memory locations would be transmitted over the data code word output channel; a 4-bit binary sector counter which defined the 16 memory word locations in the stored command delay lines; and a 4-bit binary counter which specified the memory location last filled.

The capacity of the command storage memory was increased to sixteen 40-bit words. This memory was divided into two sections designated as hot storage and cold storage. The hot storage portion contained twelve words for delayed command execution. The hot storage portion contained the remaining four words which were accessible by command only for use with other subsystems aboard the spacecraft. A fourth channel (Z channel) added to the NIMBUS C Command Clock Subsystem was used to provide the input to initiate the data code word output action.

Another change in the Command Clock was brought about by a NASA request that there be some new means of indicating that a command was stored in the memory. In NIMBUS A, the fact that a command must have been stored properly could not be verified until telemetry signified a change in the subsystem's condition as a result of that particular command being stored. To improve upon this, a provision was made in the NIMBUS C Command Clock to send a verification tone back to the Ground Station by way of the telemetry transmitter whenever a command was successfully entered into the command storage memory.

Physical characteristics of the NIMBUS C Command Clock Subsystem are shown in Table 2.

NIMBUS B Command Clock Subsystem

The NIMBUS B spacecraft is scheduled to be launched sometime during spring 1968. The Command Clock for this spacecraft is the third of the series and interfaces with nine experiments on board the spacecraft. Because of the increase in the number of experiments and because of the important role of the Command Clock, NASA specified that this Command Clock be redundant. The design objectives of the NIMBUS B Command Clock were not directed toward a more complex system and increased capability, but rather a tend toward simplifying the functional operation and increasing the reliability to ensure the probability of mission success.

To achieve redundancy and keep development costs down, CalComp used modified NIMBUS C type Command Clocks and OR'd their outputs through a third box. The third box served as an interface box and contained relays to switch the output lines of either of the two Command Clocks. Operationally, both Command Clocks are turned on during launch.

The basic individual NIMBUS B Command Clock differs from the NIMBUS C Command Clock as the result of some minor modifications. One modification was the addition of a logical mechanization to reject patterned spurious input pulses received on the three input channels. During the orbit of the NIMBUS C spacecraft, it was discovered that this type of spurious noise was occasionally being processed into the command subsystem. Another modification was the elimination of the data code words, thus enabling the stored command memory to use a full 16 words of storage for delayed command executions. With the elimination of the data code word, the Z channel input was also eliminated as the "timeout" counter function.

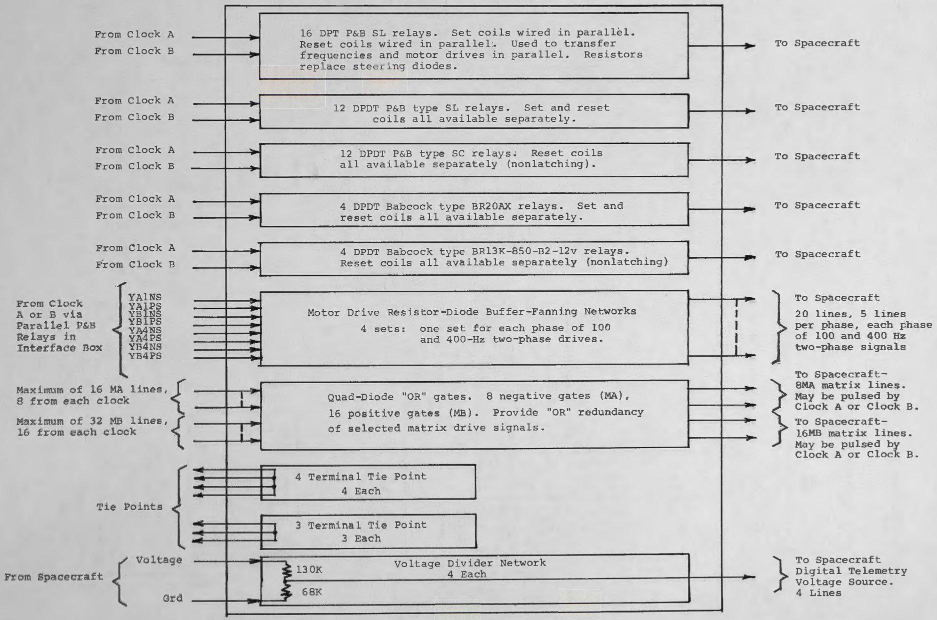
The interface box is a self-contained unit housing 48 relays mounted on twelve printed circuit boards. The relays consist of latching and non-latching types. In addition, the printed circuit boards contain discrete component OR gates for the input lines from the Command Clock Subsystems. Some of the relays can be pulsed by either Command Clock's command matrix through the OR gates. Further, for redundancy purposes, relay switching can be initiated by an unencoded command issued under Ground Station control. The signal flow diagram of the interface box is shown in Figure 7.

The two command clocks and interface box combination not only provided an increase in reliability through redundancy, but also an increase in stored commands to 32, and matrix driver fan outs to execute approximately 170 commands. The increase in the total commands which could be executed was mechanized by using particular matrix drive lines of each Command Clock Subsystem independently of each other. Redundancy on certain relay driver output lines considered to perform prime functions limited the total number of different commands to the 170 amount rather than the full 256.

Physical characteristics of the NIMBUS C Command Clock Subsystem are shown in Table 2.

FIGURE 7

NIMBUS D Command Clock Interface Box Signal Flow



NIMBUS D Command Clock Subsystem

The NIMBUS D Command Clock Subsystem is the last of the series and is presently under development. It is a new design and will interface with eleven experiments on board the spacecraft. The new design for the NIMBUS D Command Clock Subsystem is required to incorporate the changes in design objectives. Its functional objectives are the same, to process and issue timing and command signals.

The design changes require an increase in reliability to achieve an orbital life of at least one year, conformance to a standard up-data link PCM format, real time command executions, repeatability of executions initiated by stored commands, and return to a one-package subsystem.

The logic mechanization requires the use of integrated circuits, hybrid circuits, and MOS shift registers. Packaging requires the use of multilayer printed circuit boards and flexible cabling for interboard interconnections.

To achieve reliability, the NIMBUS D Command Clock Subsystem is designed to be selectively redundant. Selective redundancy refers to switching various sections of the total redundant sections to obtain a full operating subsystem. Figure 8 shows a functional block diagram of the full redundant subsystem.

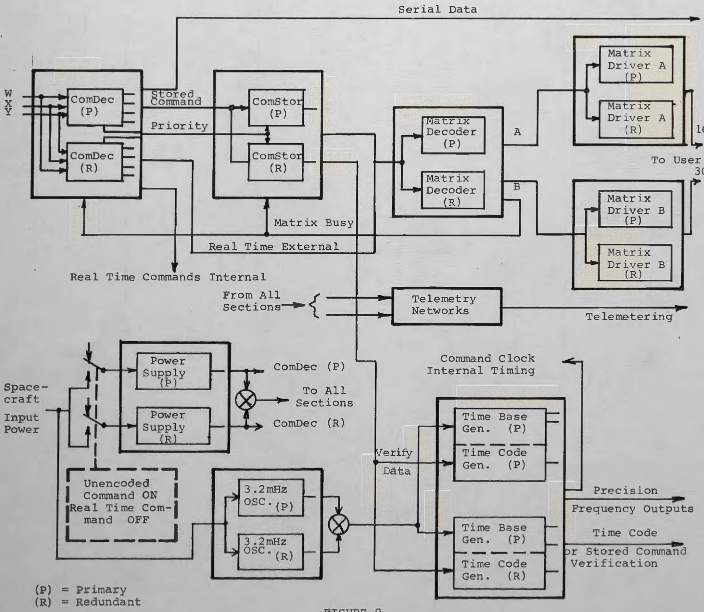


FIGURE 8

NIMBUS D Command Subsystem Functional Block

Operationally, three input channels provide the data inputs to a real time command decoder (ComDec) where all incoming data is processed. The input signal time relationship is different than that used with the other command subsystems. Figure 9 shows the relationship among the three input channels relative to the NIMBUS D Command Clock Subsystem. The W channel inputs data bits in NRZ form at the rate of 128 per second. The X channel is the W channel frequency and is positioned so that it has a positive-going transition in the middle of every data bit to provide the data strobe. The Y channel serves as a message duration pulse. The absence of the Y signal disables the ComDec input operation.

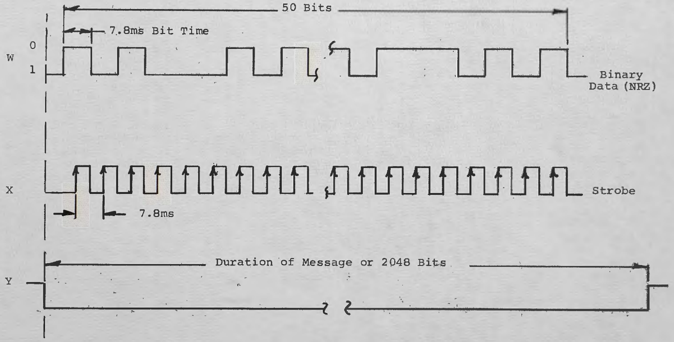


FIGURE 9

NIMBUS D Command Clock Input Waveform Relationship

There are five modes of operation pertaining to the ComDec; real time command internal, real time command external, command data storage, time code set, and serial data output. Four data input formats are required to operate in these five modes.

The real time command message format is shown in Figure 10a. The message consists of 50 bits. Twenty-five bits define the satellite address, ComDec key, operational mode and command to be executed. The remaining twenty-five bits are the complement of the preceding twenty-five bits. All bits are checked for accuracy before any action takes place. The address bits and key bits, including their complements, are compared with hard wired data bits. The mode and command bits which are captured in flip-flop registers are compared against their corresponding complementary bits. The fiftieth bit is the parity bit. If the bit-by-bit comparison and parity test pass, the command is accepted, decoded and executed.

If the bit-by-bit comparison fails, the ComDec control logic will set a telemetry error flag, reject the erroneous word and continue to accept the incoming data.

The real time command execution is initiated through the 2 x 16 matrix which is used for internal switching control or through the 16 x 30 matrix for external control. The decision as to whether the command is to be internal real time or external real time is established by the mode bits in the message.

The ComDecs are independent in that they require secondary power plus the signals from the three input channels to operate. No internal system clock is required. In addition, the ComDecs are exempt from the selective redundancy concept as each has its own power supply source which cannot be switched to work with each other. The initializing action to place a ComDec into the operational mode is to transmit an unencoded command from the Ground Station. This command activates both ComDecs. By internal real time command execution and proper ComDec identification through the key bits, one ComDec can turn the other off.

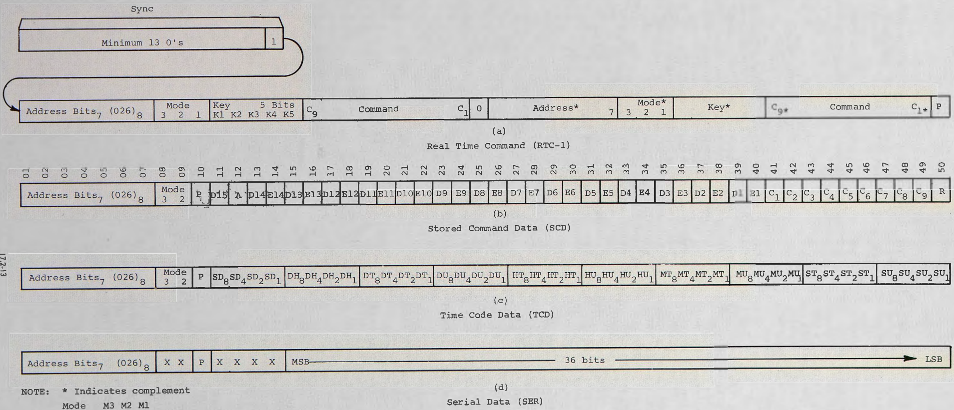
The command storage data mode transfers input data to the command storage (ComStor) section for processing and storage. The ComStor performs data storage by using dynamic type MOS shift registers which are capable of holding 50 bits of information. These shift registers are circulated at a 100-kHz rate and require a 2-phase clock for the shifting operation. There are two ComStor sections which provide the capability of 30 stored commands, 15 in each section. The ComStors are not considered to be redundant as both can be active at the same time. However, redundancy can be achieved by storing the same commands with the same time of execution in both ComStors.

The command data format message sent to the ComStor is shown in Figure 10b. Only bits 11 through 50 have any real significance. The 15 D bits contain the time for command execution; the 14 E bits determine the repeat time; and the C bits hold the command to be executed. The R and A bits are used to establish if a command is to be repeated or not. The address and mode bits are used for a message validity check by the ComDec section only.

The D bits are decremented at the rate of once every two seconds and then tested for zero (the condition which will cause the command to be executed). If R is "one" and A is "one," the repeat time held in the E bit position is rewritten into the corresponding bit position of the D positions. If R is "zero" and A is "one", then the command is executed one time. Because the D bits are decremented once every two seconds, 15 bits will provide up to 18 hours delay. If the repeat bit is used, then delays can be repeated at intervals up to nine hours.

Each of the two ComStors are individually controlled. Their MOS registers can be sequentially or selectively filled, have their contents verified, be placed in an activate mode for command delayed executions or be completely inoperative by turning off their power supplies. The ComStor operating modes are initiated under real time command control issued by the ComDec. In the fill mode, the fill counter is reset to service the MOS registers. As each device is loaded the counter is incremented. However, if a MOS register contains information that is to be retained, a real time command is issued which increments the counter to skip that register and preserve its contents. The verify mode allows each MOS register to be interrogated, formatted in the time code data format, and transmitted to the Ground Station at the rate of one word per second for comparison with command storage data initially transmitted. The time portion of the stored data is decremented once every two seconds during the verify mode to preserve the time of stored command execution. However, during this mode no commands will be executed should any register happen to be all zeros. The activate mode enables the ComStor to issue a command each time a MOS register is decremented to zero provided that the A bit is a "one." All ComStor commands to be issued are sent to the matrix decoder/driver section for execution.

The matrix decoder/driver section receives commands for execution from the ComDec or either of the two ComStors. To solve the race to the matrix problem, the ComDec is given priority over the ComStors and each ComStor is time phased so that only one ComStor section can output commands at a particular second. If a ComStor is ready to issue a command, and a real time command is being processed in the ComDec, the ComStor command will be held up until the real time command is executed.



NOTE: * Indicates complement

Mode	M3	M2	M1	
	1	1	1	Real Time Command External (RTCE)
	1	1	0	Real Time Command Internal (RTCI)
	0	1	-	Stored Command Data (SCD)
	1	0	-	Time Code Data (TCD)
	-	-	-	Serial Data (SER)

FIGURE 10

NIMBUS D Command Word Formats

The matrix decode driver section performs the same function as the other Command Subsystems. However, it is mechanized with hybrid circuit type relay drivers. The matrix is 16 x 30 to execute 480 commands. The matrix is redundant and because of the redundant driver mechanization, the spacecraft has four chances of executing each particular command. The time duration for any command execution is 53 milliseconds. In two seconds, it is possible to execute all stored commands plus two real time commands.

The third operating mode of the ComDec is to transfer a time code set message to the time code generation section. The time code generation section performs two functions. It provides real time and generates the precision frequencies for the spacecraft subsystems. Time code data is generated in conjunction with a 50-bit MOS shift register which contains 10 BCD characters signifying time from one second increments, the smallest, to hundreds of days, the largest. If the time code register is to be updated, a time set code message consisting of the format shown in Figure 10c is processed through ComDec and stored in the time code data MOS register which can be commanded to a fill mode. The time code data format uses only 40 bits, 11 through 50 inclusively, for time processing.

The time code generation section divides the signal from the 3.2-mHz oscillator to generate the various coherent precision frequencies for other subsystems. Signal division is accomplished with flip-flop ripple counters whereas synchronous flip-flop operation was used in the preceding NIMBUS Command Clock Subsystems. The integrated circuit ripple counters are much faster than their discrete component counterparts; therefore, synchronous clocking is not necessary to keep the signals coherent.

The last mode of operation for the ComDec is the serial data transfer mode. The serial data transfer mode is associated with another subsystem on the spacecraft. The serial data mode format is shown in Figure 10d. The ComDec switches the receiving subsystem into its data input mode. As the serial data is transmitted to the spacecraft, the ComDec receives, checks the address, parity and key bits. These items are stripped out and only the 36 data bits are sent to the subsystem. The ComDec has been designed not to interrupt this serial data transmission mode under any circumstances. Therefore, during the checking portion of the input word, if an error is detected, a flag is set and telemetered back to the Ground Station. The only manner in which the Command Clock Subsystem can be taken out of the serial data mode is to drop the Y input pulse which resets the ComDec to the look-for-sync-word condition.

The other sections shown in the block diagram contain the secondary power levels, telemetry networks, and amplifiers.

Physical characteristics pertaining to the NIMBUS D Command Clock Subsystem are shown in Table 2.

Conclusion

The evolutionary process of the NIMBUS Command Clock Subsystems has progressed from the single box, non-redundant, discrete component type to a three box, dual-redundant, discrete component type and back to a single box, selectively redundant, state-of-the-art component type. The trend has been to provide more capability into the same or less space, exhibit a high probability of successful operation and provide system flexibility for additions or delections without going through a full design and development program. The NIMBUS D Command Clock Subsystem is designed to meet these requirements.